IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	Mukul R. Prasad et al.
Date Filed:	March 23, 2004
Title:	*Scheduling Events in a Boolean Satisfiability (SAT) Solver*

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Dear Sir:

INFORMATION DISCLOSURE STATEMENT

Under 37 C.F.R. §§ 1.56, .97, and .98, Applicants respectfully request that the references listed in the attached PTO-1449 form be considered and cited in the examination of the Application. The present Application was filed after June 30, 2003. Therefore, under the July 11, 2003, waiver of 37 C.F.R. § 1.98(a)(2)(i) by the U.S. Patent and Trademark Office, copies of U.S. Patents and U.S. Patent Application Publications listed in the attached PTO-1449 form are not enclosed. Copies of all other references are enclosed for the convenience of the Examiner.

Respectfully submitted,

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PTO-1449 **Information Disclosure Citation in an Application**	**Application No.**	**Applicant(s)** **Mukul R. Prasad et al.**	
	Docket Number **073338.0172** **(03-52027 FLA)**	**Group Art Unit**	**Filing Date** **March 23, 2004**

U.S. PATENT DOCUMENTS

		DOCUMENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE
	A						
	B						
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	E						

FOREIGN PATENT DOCUMENTS

		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
	F							
	G							

NON-PATENT DOCUMENTS

		DOCUMENT (Including Author, Title, Source, and Pertinent Pages)	DATE
	H	Marques-Silva et al., "GRASP: A Search Algorithm for Propositional Satisfiability," IEEE Trans. on Computers, vol. 48, No. 5, pp. 506-521, May 1999.	May 1999
	I	Moskewicz et al., "Chaff: Engineering an Efficient SAT Solver," in Proc. of the 38th Design Automation Conference, June 2001, pp. 530-535.	June 2001
	J	Zhang et al., "SATO: An Efficient Propositional Prover," in Proc. of the International Conference on Automated Deduction, July 1997, pp. 272-275.	July 1997
	K	Goldberg et al., "BerkMin: a Fast and Robust Sat-Solver," in Proc. of Design and Test in Europe, March 2002, pp. 142-149.	March 2002
	L	Stephen et al., "Combinational Test Generation Using Satisfiability," IEEE Trans. on CAD, vol. 15, no. 9, pp. 1167-1176, September 1996.	September 1996
	M	Biere et al., "Symbolic Model Checking without BDDs," in Proc. of TACAS'99, March 1999, pp. 193-207.	March 1999
	P	Bryant, et al., "Processor Verification Using Efficient Reductions of the Logic of Uninterpreted Functions to Propositional Logic," ACM Trans. on Computational and Sequential Logic, vol. 2. no. 1, pp. 1-41, January 2001.	January 2001
	Q	Entrena et al., "Combinational and Sequential Logic Optimization by Redundancy Addition and Removal," IEEE Trans. on CAD, vol. 14, no. 7, pp. 909-916, July 1995.	July 1995
	R	Wood et al., "FPGA Routing and Routability Estimation via Boolean Satisfiability," IEEE Trans. on VLSI, vol. 6, no. 2, pp. 222-231, June 1998.	June 1998
	S	Davis et al., "A Machine Program for Theorem-Proving," Communications of the ACM, vol. 5, pp. 394-397, July 1962.	July 1962

EXAMINER	**DATE CONSIDERED**

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.